

ABSTRACT OF THE DISCLOSURE

A layout structure of a decoder with $m \times n$ nodes and the method thereof are provided. The nodes comprise a plurality of transistor nodes and a plurality of channel nodes. The manufacturing method of the transistor node comprises forming a gate, a first source/drain region and a second source/drain region. The channel node is fabricated by forming a channel. The channel, the first source/drain region and the second source/drain region are formed at the same time with the same material. The decoder circuit with smaller width is accomplished without additional mask in the invention.

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